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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/013,087	12/07/2001	Hideyuki Andoh	44471-267680 (13700)	1427
23370	7590	10/06/2004	EXAMINER	
JOHN S. PRATT, ESQ KILPATRICK STOCKTON, LLP 1100 PEACHTREE STREET ATLANTA, GA 30309				SCHILLINGER, LAURA M
ART UNIT		PAPER NUMBER		
				2813

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/013,087	ANDOH, HIDEYUKI <i>[Signature]</i>
	Examiner	Art Unit
	Laura M Schillinger	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 22 July 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-9 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-9 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the phrase “common tangent plane” fails to exist within the specification. More specifically there is no disclosure within the specification of the limitations of claim 1 which recite “a second semiconductor region … so as to have **the lower end surface as a common tangent plane between the first and second semiconductor region**” and “a third semiconductor region…so as to have **the upper end surface as a common tangent plane between the first and third semiconductor regions**”. If such disclosure exists within the Figures, Applicant can overcome this rejection by providing an explanation as to how the figures depict this claim language; the Examiner reviewed the drawings and could not find a showing of the above claimed limitations. Applicant has therefore added new matter into the claims which is not supported by the original specification as filed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Jambotkar ('857).

In reference to claim 1, Jambotkar teaches a device comprising:

A first semiconductor region of a first conductivity type, defined by an upper end surface and a side boundary surface connecting the upper and lower end surfaces when viewed in section (Fig.2A (16));

A second semiconductor region of the first conductivity type in metallurgical contact (s1) with the first semiconductor region at the lower end surface (Fig.2A (14));

A third semiconductor region of a second conductivity type metallurgical contact (B1) with the first semiconductor region at the upper end surface (Fig.2A (12)); and

A fourth semiconductor region having inner surface in metallurgical contact (W1) with the side boundary surface when viewed in section and an impurity concentration lower than the first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions (Fig.2A (10)).

In reference to claim 2, Jambotkar teaches wherein the fourth semiconductor region has a first type conductivity (Fig.2A (10)).

In reference to claim 3, Jambotkar teaches wherein outer surface of the fourth semiconductor region serves as a chip outer surface of the semiconductor device and the chip outer surface is substantially orthogonal with the lower end surface of the first semiconductor region.

In reference to claim 4, Jambotkar teaches wherein the fourth semiconductor region is made of a wafer cut from bulk crystal (Fig.2A (10) and Col.7, lines: 15-20).

In reference to claim 5, Jambotkar teaches further comprising a first main electrode layer is formed on a bottom surface of the second semiconductor region (Fig.2A (S1)).

In reference to claim 6, Jambotkar teaches wherein the first main electrode layer is contacted with the second semiconductor region, through a first concavity formed at the bottom surface of the second semiconductor region (Fig.3 (20')).

In reference to claim 7, Jambotkar teaches further comprising a first main electrode layer, a part of the first main electrode layer is buried in a via hole penetrating through the second semiconductor region, configured such that the buried part of the first main electrode layer contacts with the first semiconductor region (Fig.2A (S1)).

In reference to claim 8, Jambotkar teaches further comprising a second main electrode layer is formed on a top surface of the third semiconductor region (Fig.4A (G1)).

In reference to claim 9, Jambotkar teaches wherein the second main electrode layer is contacted with the first semiconductor regions, through a second concavity formed at the top surface of the third semiconductor region (Fig.3 (20')).

Response to Arguments

Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection. Applicant argues that Jambotkar fails to teach his newly added claim language. However, such an argument is not persuasive because the claim language is not supported by the specification. **Applicant is hereby requested to provide page, line citations and drawing reference numeral citations for all future amendments made in prosecution of the case to expedite prosecution and prevent the inadvertent addition of new matter.**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2813

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMS

9/25/04